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MS-7610

Version 2.1

CPU:

Intel Conroe (95W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)

Intel ICH7 (South Bridge)

On Board Chipset:

BIOS -- SPI

HD -- RTL889

LPC Super I/O -- F71889G

LAN - 8111DL

CLOCK -- RTM875-605

Main Memory:

DDR III *2 (Max 4GB)

Expansion Slots:

PCI2.3 SLOT * 3

PCI EXPRESS X1 SLOT *2

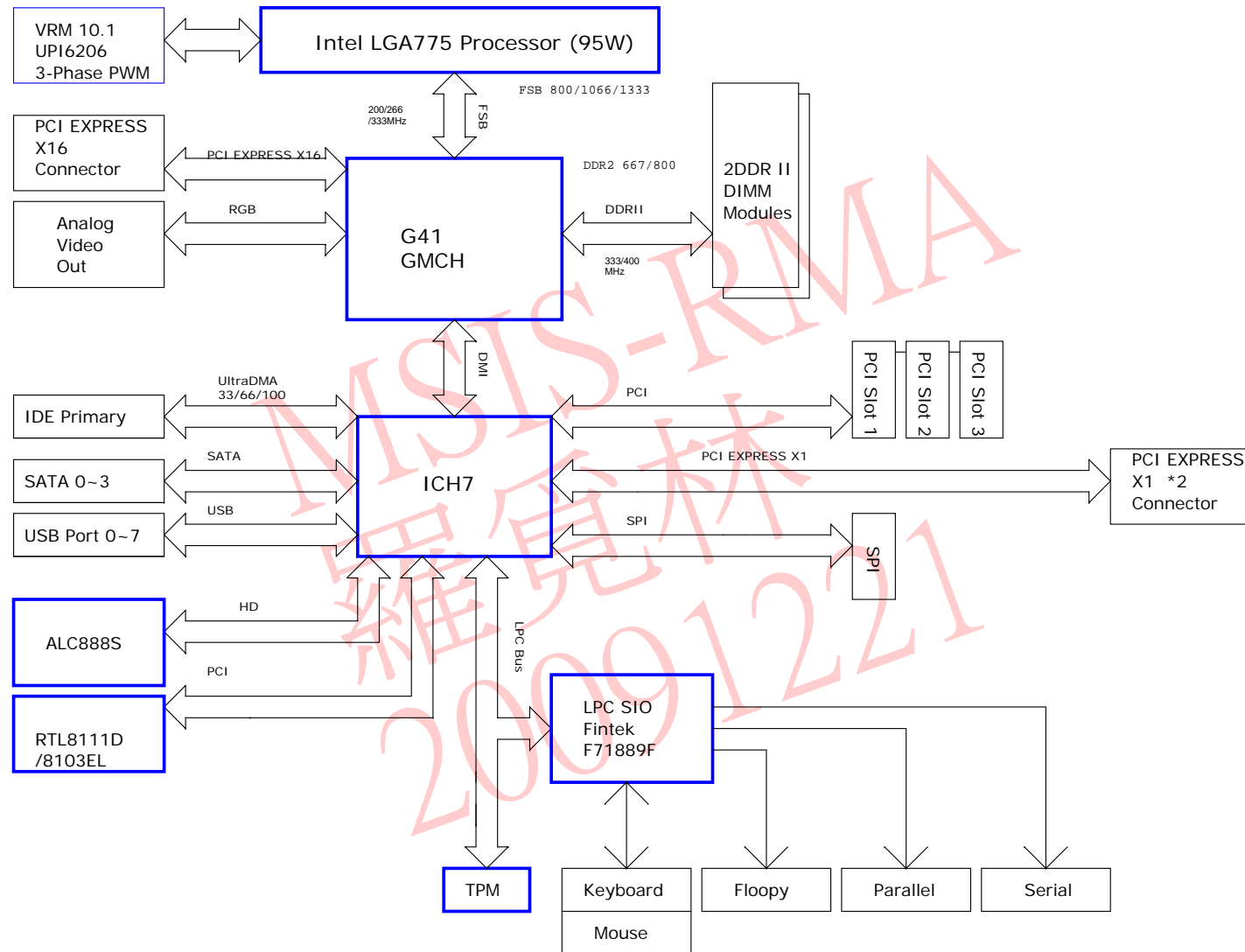
PCI EXPRESS X16 SLOT *1

UPI PWM:

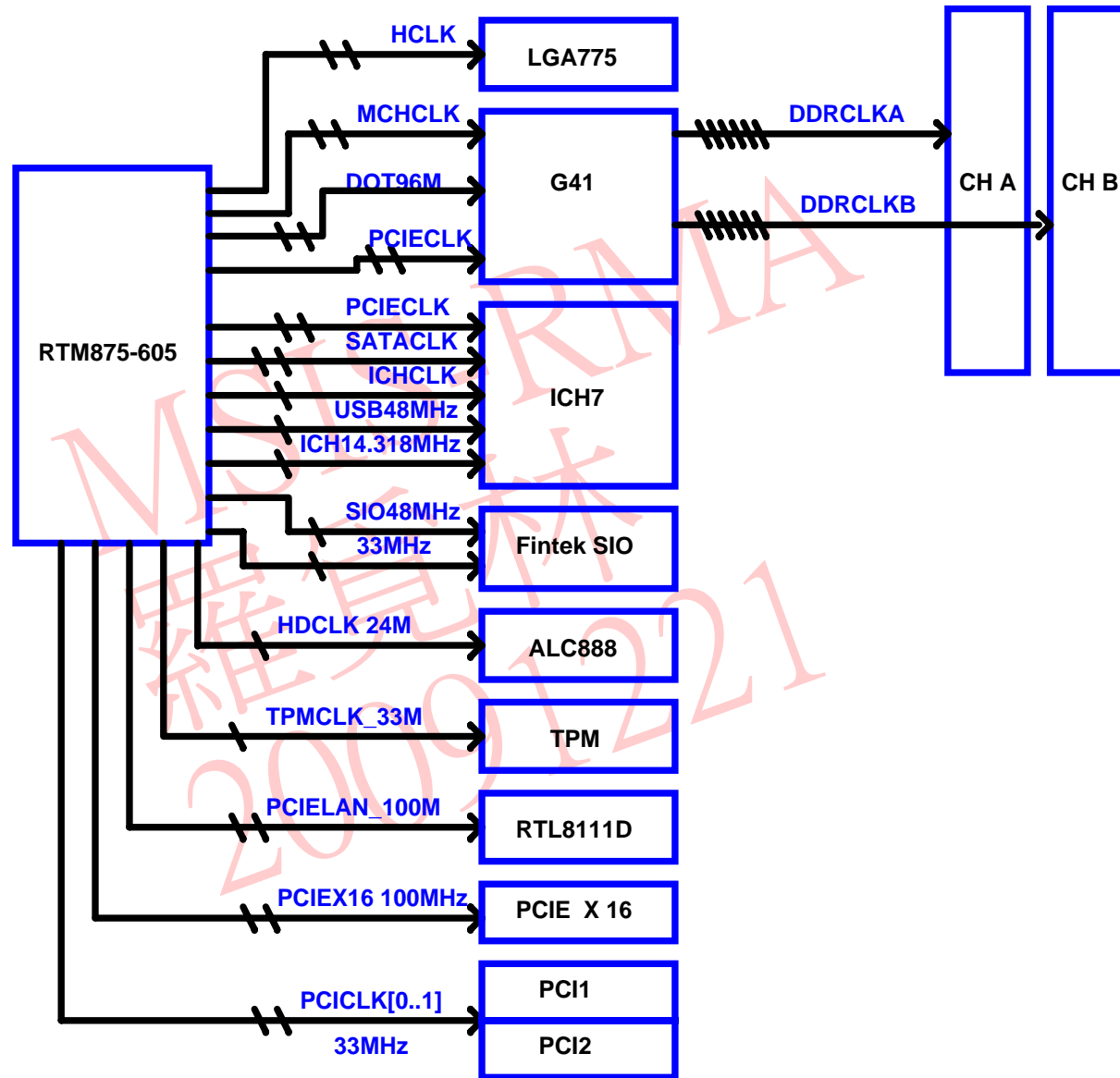
Controller: 3 PHASES + APS

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Block Diagram



CLOCK MAP



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Processor (95W)
1.15-1.5000V Core-70A
1.2V FSB Vtt-5.8A
VCCPLL
VCC-IOPLL & VCCA

G41 MCH 1.1V core 22A
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.1V Core-13.8A(Integrated)
1.1V Core-8.9A(Discrete)
1.5V PCI Express&DMI-0.68A
1.1V PCIE&DMI PLL-41mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
1.1V Vcc-core 1.16A
1.1V VCC_CL-3A

ICH7
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5 SATA/USB/PLL 1.65A
VCC1_5B*-0.646A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-41mA
VccSATAIPLL-50mA

Battery

UPI6206 Regulator
VCCP
1.15-1.5000V

VTT Regulator
V_FSB_VTT
1.2V

uP6103 Regulator
VCC_DDR
1.8V

V1.5 Regulator
V_1P5_CORE
1.5V

1.1V Regulator
V_1P1_Core
1.1V

1.05V Regulator
V_1P05_CORE
1.05V

uP7706 Regulator
3VSB
3.3V

uP7501 Regulator
5VDIMM
5V

W83310DS Regula
VTT_DDR
0.9V

DDR2 DIMM conn(4) & term
0.9V SM Vtt-1.2A(S0)
1.8V Vdd/vddq-4.7A(S0,S1)

PCIE X16 slot(1)
+12V-5.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCIE X1 slot(0)
+12V-0.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCI slot slot(2)
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-5.6A
+5.0V-5.0A
+12V-0.5A
-12V-0.1A

USB
+5V-4A(S0,S1)

PS2
+5V-345mA(S0,S1)

CLKGEN
+3.3V-560mA

LAN
3VSB-

SIO
+3.3V
3VSB-

SPI ROM

Audio Codec

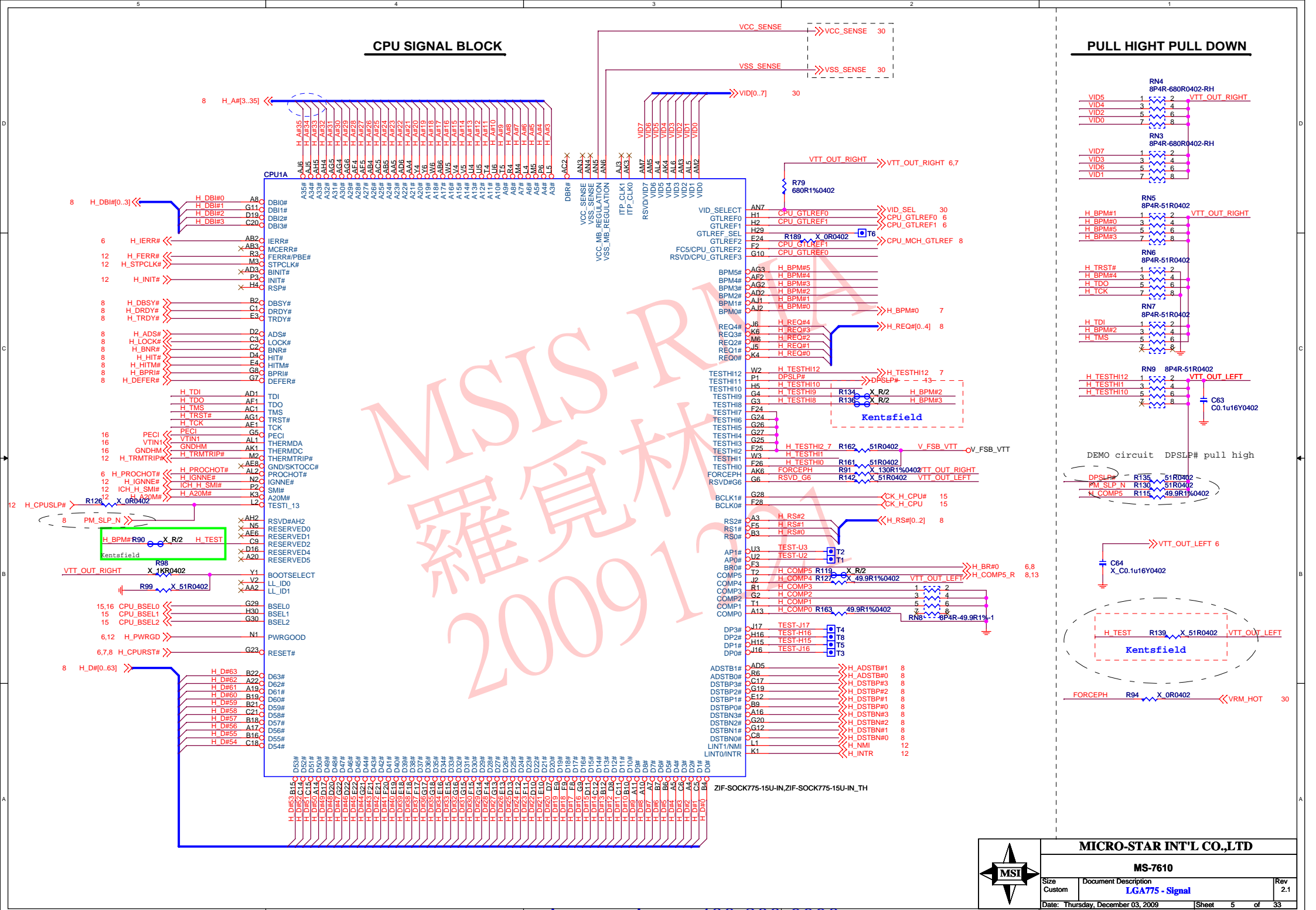
1394

+12V
ATX 2x2

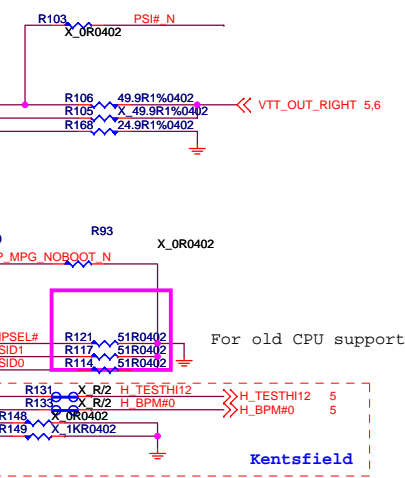
+12V	+5V	+3.3V	+5VSB
ATX POWER			

CPU SIGNAL BLOCK

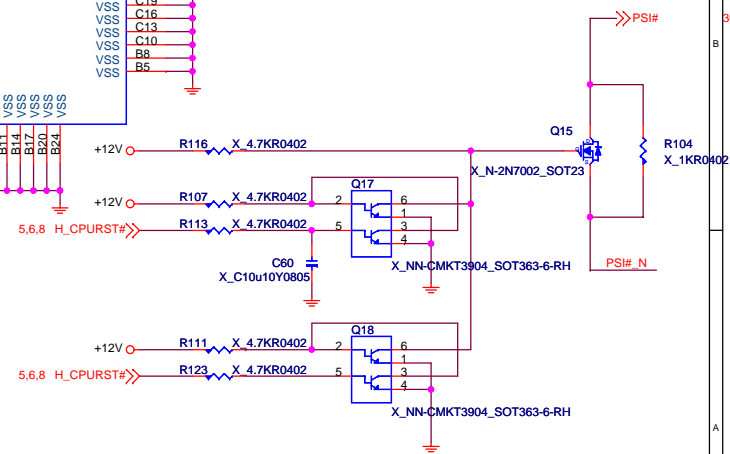
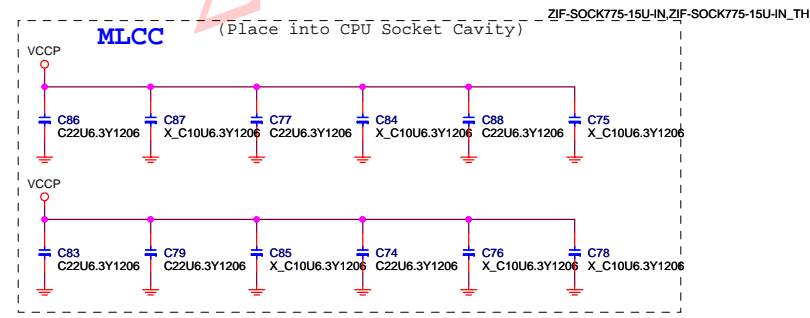
PULL HIGH PULL DOWN



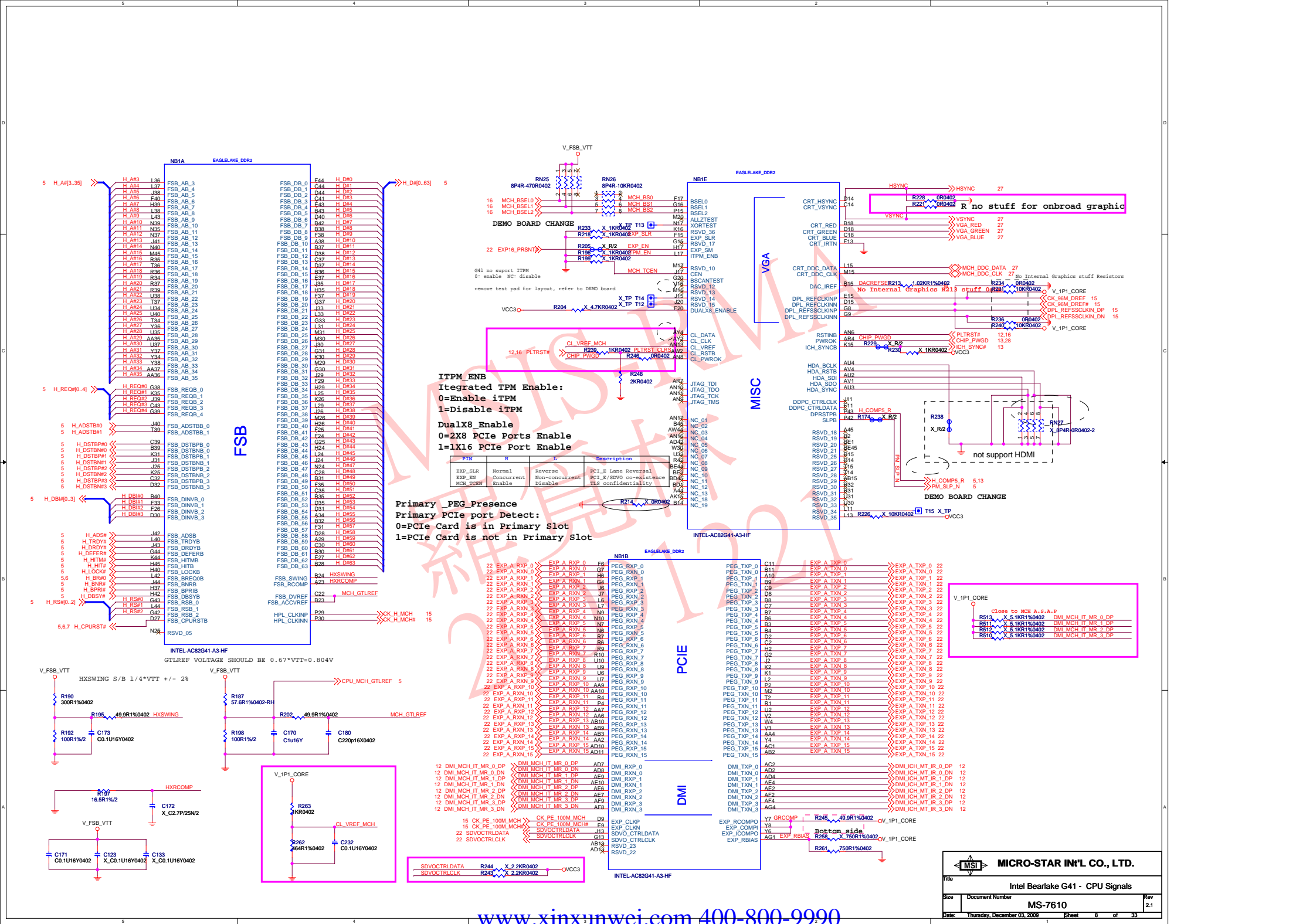
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Custom	LGA775 - Signal	2.1	
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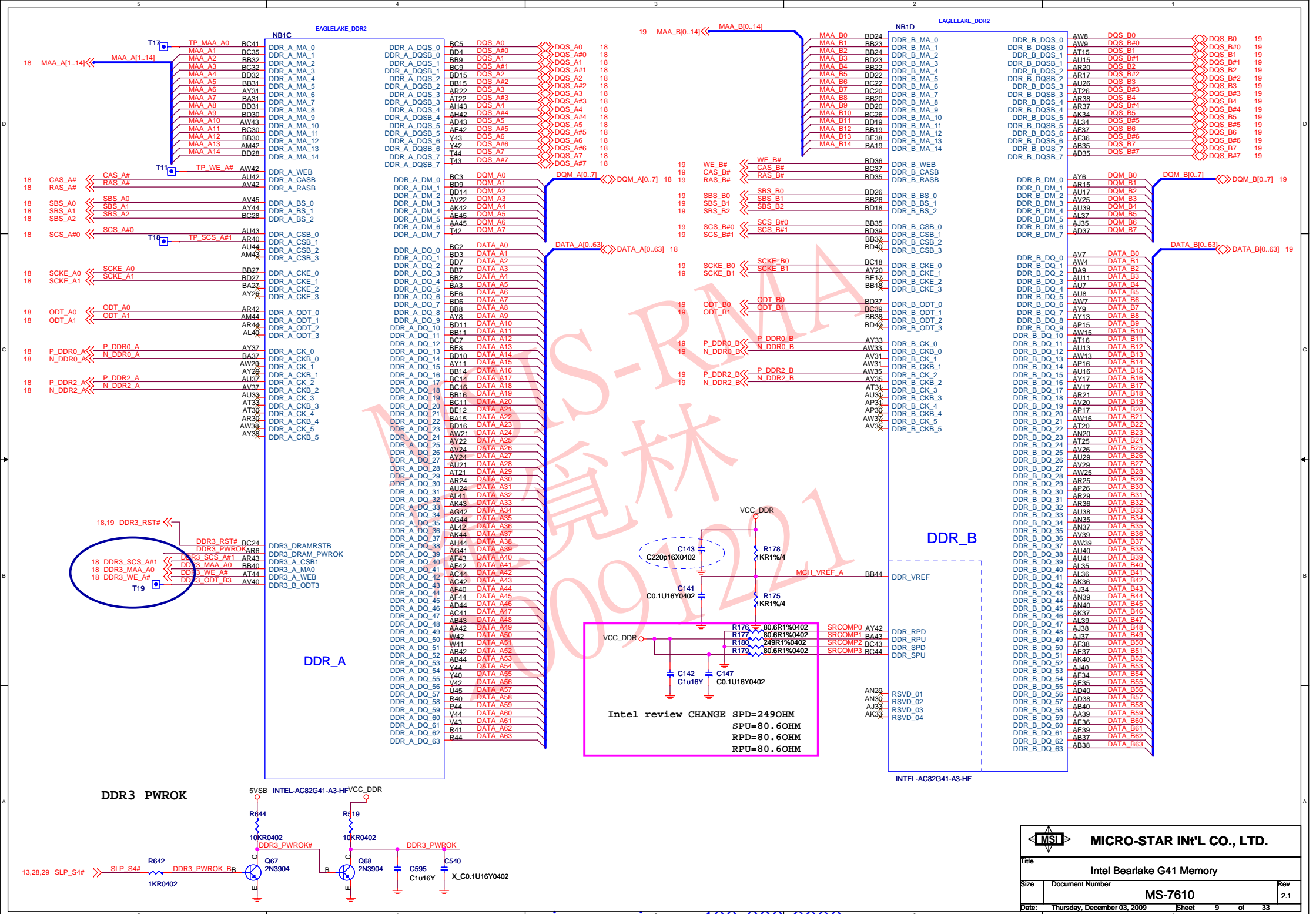


	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1



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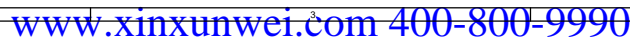
NB1G



GND

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 MICRO-STAR INT'L CO., LTD.		
Title Intel Bearlake G41 GND		
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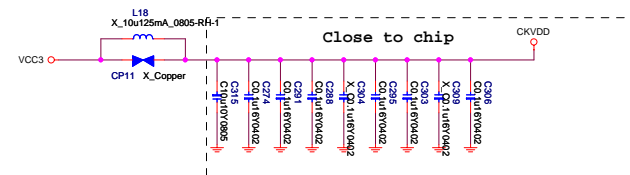
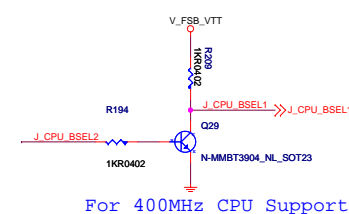
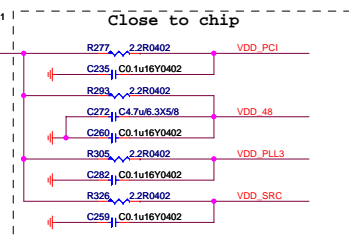
The diagram shows the pin-to-pin connections for the RTM8751-605-VD-R (TSSOP56) package. The left side lists the package pins (1-56) and their functions. The right side lists the corresponding CPU0-# pins (1-56) and their functions. The connections are as follows:

Package Pin	Package Function	CPU0-# Pin	CPU0-# Function
1	VDD_PCI	46	CK_H_CPU#
2	VDD_PCI	47	CK_H_CPU#
3	VDD_PLL3	48	CK_H_CMH#
4	VDD_PLL3	49	CK_H_CMH#
5	VDD_SRC	50	CK_H_CMH#
6	VDD_SRC	51	CK_H_CMH#
7	VDD_SRC	52	CK_H_CMH#
8	VDD_SRC	53	CK_H_CMH#
9	VDD_SRC	54	CK_H_CMH#
10	VDD_SRC	55	CK_H_CMH#
11	VDD_SRC	56	CK_H_CMH#
12	VDD_SRC	57	CK_H_CMH#
13	VDD_SRC	58	CK_H_CMH#
14	VDD_SRC	59	CK_H_CMH#
15	VDD_SRC	60	CK_H_CMH#
16	VDD_SRC	61	CK_H_CMH#
17	VDD_SRC	62	CK_H_CMH#
18	VDD_SRC	63	CK_H_CMH#
19	VDD_SRC	64	CK_H_CMH#
20	VDD_SRC	65	CK_H_CMH#
21	VDD_SRC	66	CK_H_CMH#
22	VDD_SRC	67	CK_H_CMH#
23	VDD_SRC	68	CK_H_CMH#
24	VDD_SRC	69	CK_H_CMH#
25	VDD_SRC	70	CK_H_CMH#
26	VDD_SRC	71	CK_H_CMH#
27	VDD_SRC	72	CK_H_CMH#
28	VDD_SRC	73	CK_H_CMH#
29	VDD_SRC	74	CK_H_CMH#
30	VDD_SRC	75	CK_H_CMH#
31	VDD_SRC	76	CK_H_CMH#
32	VDD_SRC	77	CK_H_CMH#
33	VDD_SRC	78	CK_H_CMH#
34	VDD_SRC	79	CK_H_CMH#
35	VDD_SRC	80	CK_H_CMH#
36	VDD_SRC	81	CK_H_CMH#
37	VDD_SRC	82	CK_H_CMH#
38	VDD_SRC	83	CK_H_CMH#
39	VDD_SRC	84	CK_H_CMH#
40	VDD_SRC	85	CK_H_CMH#
41	VDD_SRC	86	CK_H_CMH#
42	VDD_SRC	87	CK_H_CMH#
43	VDD_SRC	88	CK_H_CMH#
44	VDD_SRC	89	CK_H_CMH#
45	VDD_SRC	90	CK_H_CMH#
46	VDD_SRC	91	CK_H_CMH#
47	VDD_SRC	92	CK_H_CMH#
48	VDD_SRC	93	CK_H_CMH#
49	VDD_SRC	94	CK_H_CMH#
50	VDD_SRC	95	CK_H_CMH#
51	VDD_SRC	96	CK_H_CMH#
52	VDD_SRC	97	CK_H_CMH#
53	VDD_SRC	98	CK_H_CMH#
54	VDD_SRC	99	CK_H_CMH#
55	VDD_SRC	100	CK_H_CMH#
56	VDD_SRC	101	CK_H_CMH#

Additional connections shown in the diagram include:

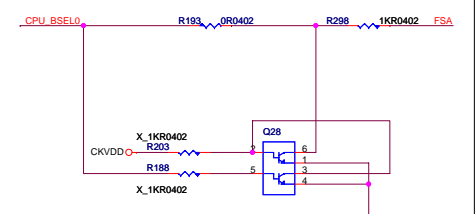
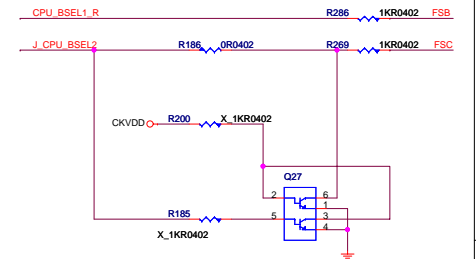
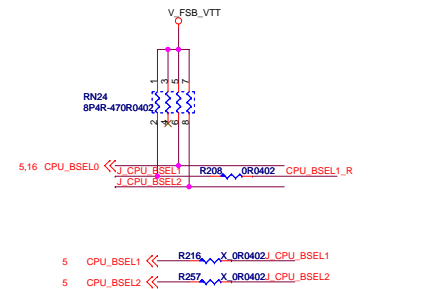
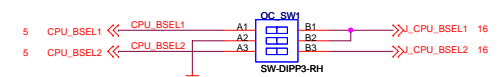
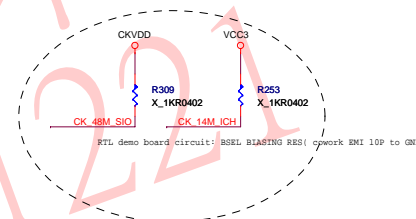
- Pin 12 (VDD_SRC) to Pin 13 (CK_H_CMH#)
- Pin 13 (CK_H_CMH#) to Pin 14 (CK_H_CMH#)
- Pin 14 (CK_H_CMH#) to Pin 15 (CK_H_CMH#)
- Pin 15 (CK_H_CMH#) to Pin 16 (CK_H_CMH#)
- Pin 16 (CK_H_CMH#) to Pin 17 (CK_H_CMH#)
- Pin 17 (CK_H_CMH#) to Pin 18 (CK_H_CMH#)
- Pin 18 (CK_H_CMH#) to Pin 19 (CK_H_CMH#)
- Pin 19 (CK_H_CMH#) to Pin 20 (CK_H_CMH#)
- Pin 20 (CK_H_CMH#) to Pin 21 (CK_H_CMH#)
- Pin 21 (CK_H_CMH#) to Pin 22 (CK_H_CMH#)
- Pin 22 (CK_H_CMH#) to Pin 23 (CK_H_CMH#)
- Pin 23 (CK_H_CMH#) to Pin 24 (CK_H_CMH#)
- Pin 24 (CK_H_CMH#) to Pin 25 (CK_H_CMH#)
- Pin 25 (CK_H_CMH#) to Pin 26 (CK_H_CMH#)
- Pin 26 (CK_H_CMH#) to Pin 27 (CK_H_CMH#)
- Pin 27 (CK_H_CMH#) to Pin 28 (CK_H_CMH#)
- Pin 28 (CK_H_CMH#) to Pin 29 (CK_H_CMH#)
- Pin 29 (CK_H_CMH#) to Pin 30 (CK_H_CMH#)
- Pin 30 (CK_H_CMH#) to Pin 31 (CK_H_CMH#)
- Pin 31 (CK_H_CMH#) to Pin 32 (CK_H_CMH#)
- Pin 32 (CK_H_CMH#) to Pin 33 (CK_H_CMH#)
- Pin 33 (CK_H_CMH#) to Pin 34 (CK_H_CMH#)
- Pin 34 (CK_H_CMH#) to Pin 35 (CK_H_CMH#)
- Pin 35 (CK_H_CMH#) to Pin 36 (CK_H_CMH#)
- Pin 36 (CK_H_CMH#) to Pin 37 (CK_H_CMH#)
- Pin 37 (CK_H_CMH#) to Pin 38 (CK_H_CMH#)
- Pin 38 (CK_H_CMH#) to Pin 39 (CK_H_CMH#)
- Pin 39 (CK_H_CMH#) to Pin 40 (CK_H_CMH#)
- Pin 40 (CK_H_CMH#) to Pin 41 (CK_H_CMH#)
- Pin 41 (CK_H_CMH#) to Pin 42 (CK_H_CMH#)
- Pin 42 (CK_H_CMH#) to Pin 43 (CK_H_CMH#)
- Pin 43 (CK_H_CMH#) to Pin 44 (CK_H_CMH#)
- Pin 44 (CK_H_CMH#) to Pin 45 (CK_H_CMH#)
- Pin 45 (CK_H_CMH#) to Pin 46 (CK_H_CMH#)
- Pin 46 (CK_H_CMH#) to Pin 47 (CK_H_CMH#)
- Pin 47 (CK_H_CMH#) to Pin 48 (CK_H_CMH#)
- Pin 48 (CK_H_CMH#) to Pin 49 (CK_H_CMH#)
- Pin 49 (CK_H_CMH#) to Pin 50 (CK_H_CMH#)
- Pin 50 (CK_H_CMH#) to Pin 51 (CK_H_CMH#)
- Pin 51 (CK_H_CMH#) to Pin 52 (CK_H_CMH#)
- Pin 52 (CK_H_CMH#) to Pin 53 (CK_H_CMH#)
- Pin 53 (CK_H_CMH#) to Pin 54 (CK_H_CMH#)
- Pin 54 (CK_H_CMH#) to Pin 55 (CK_H_CMH#)
- Pin 55 (CK_H_CMH#) to Pin 56 (CK_H_CMH#)

The diagram also shows the connection of the package pins to the CPU0-# pins, with the package pins numbered 1 to 56 and the CPU0-# pins numbered 1 to 56. The package pins are labeled with their functions, and the CPU0-# pins are labeled with their functions. The connections are shown as lines between the package pins and the CPU0-# pins.



	0	1
TIME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
ITP_EN	Pin38/39 is SRC 8	Pin38/39 is CPUITP

Default	200-->266	200-->333	200-->400
1:ON	1:ON	1:ON	1:OFF/ON
2:OFF	2:ON	2:ON	2:OFF
3:ON	3:ON	3:OFF	3:OFF
		266-->333	266-->400
		1:ON	1:OFF
		2:OFF	2:OFF
		3:OFF	3:OFF
			333-->400
			1:OFF
			2:OFF
			3:OFF

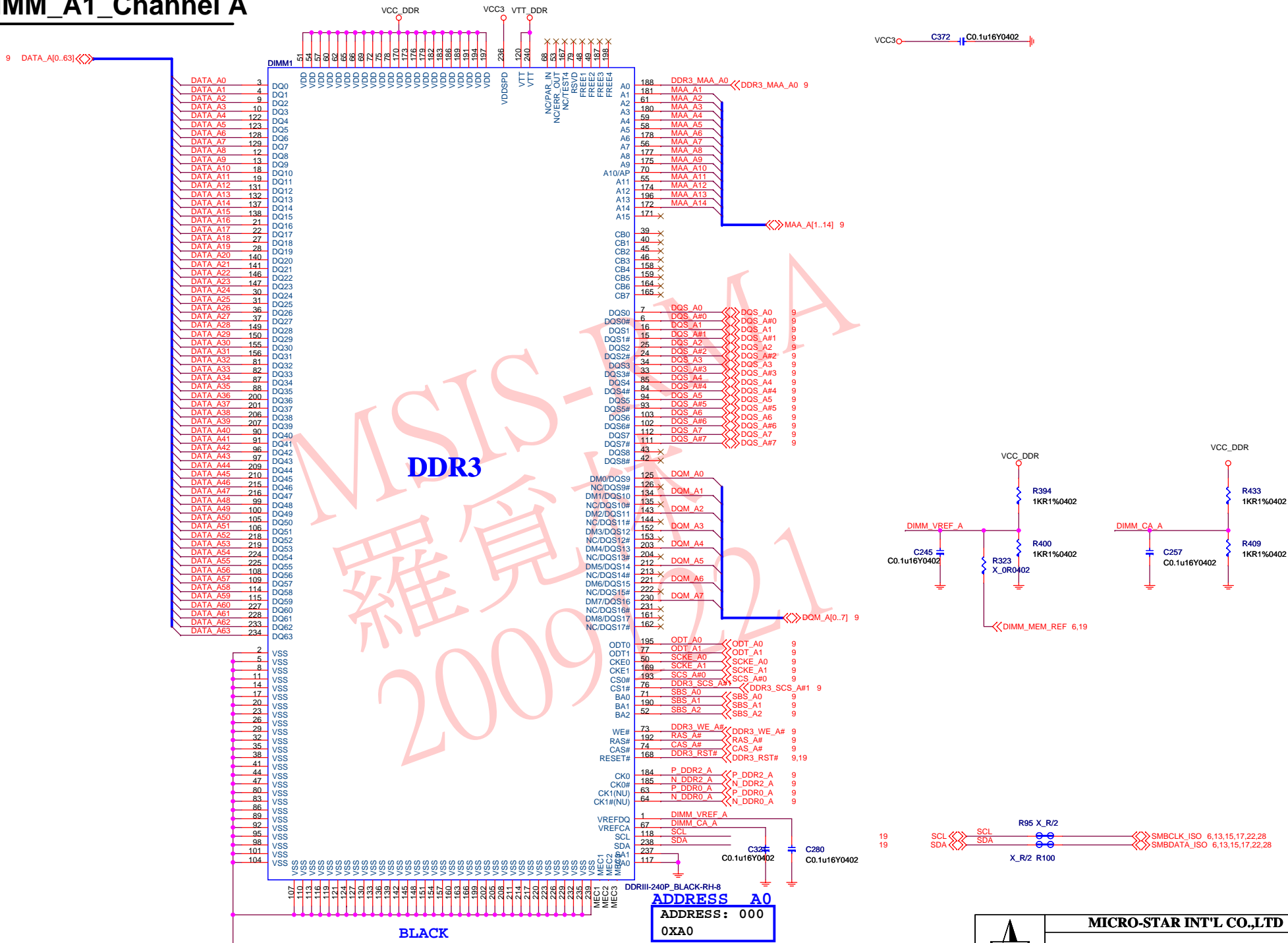


FS_C	FS_B	FS_A	CPU
0	0	1	133%
0	1	0	200%
0	0	0	266%
1	0	0	333%
1	1	0	400%



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DDR II DIMM_A1_Channel A



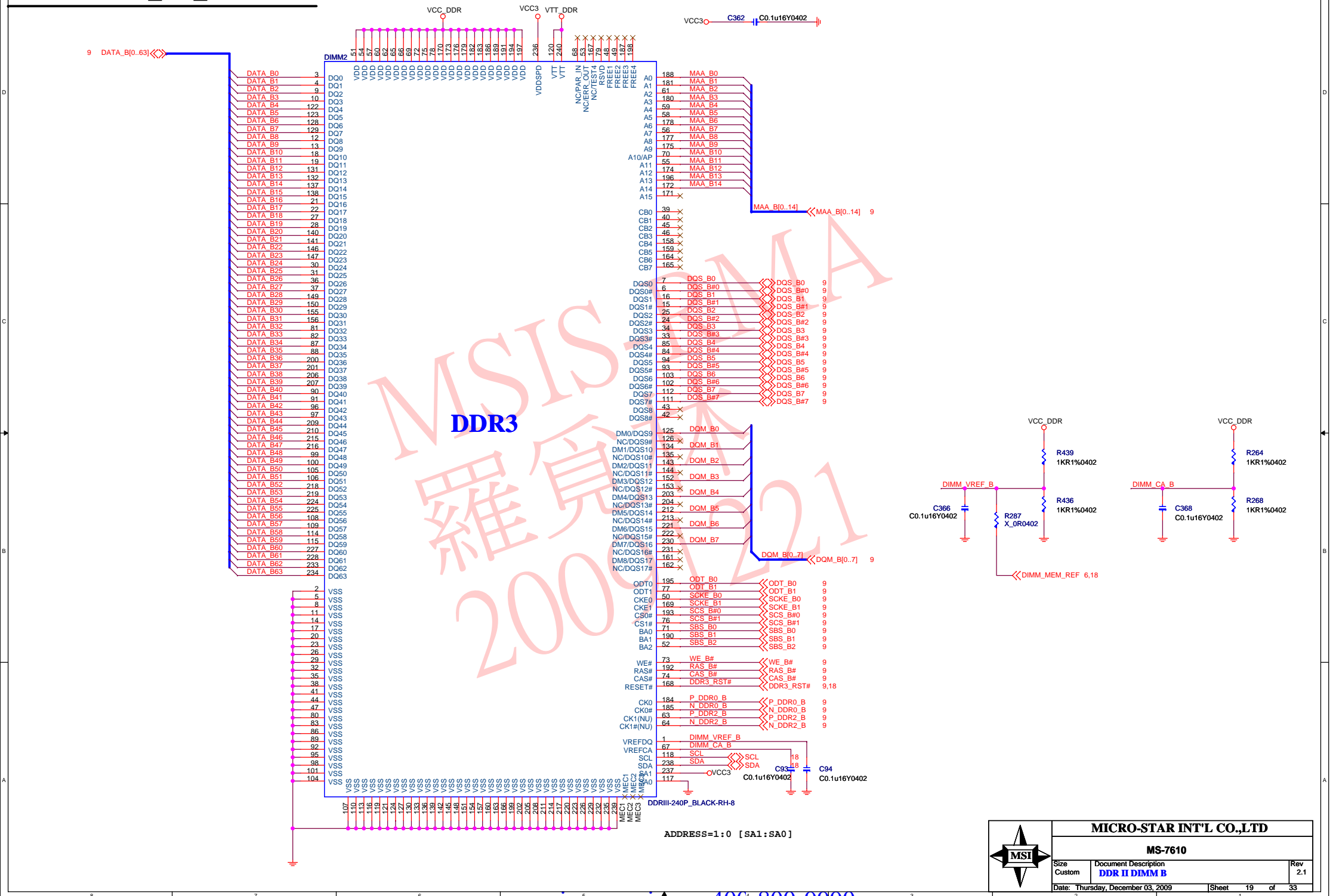
DDR3

ADDRESS A0
ADDRESS: 000
0XA0

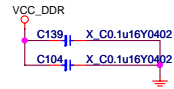
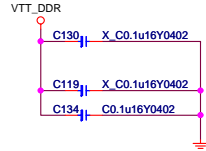
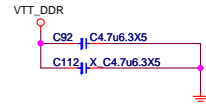
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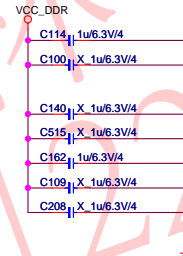
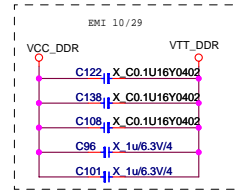
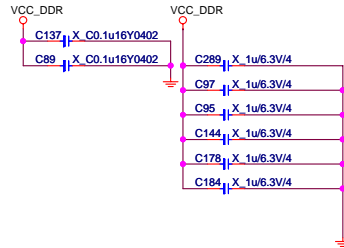
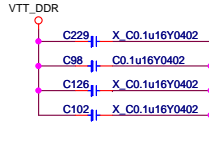
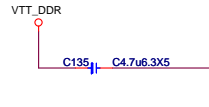
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CHANNEL A V_SM_VTT DECOUPLING CAPS

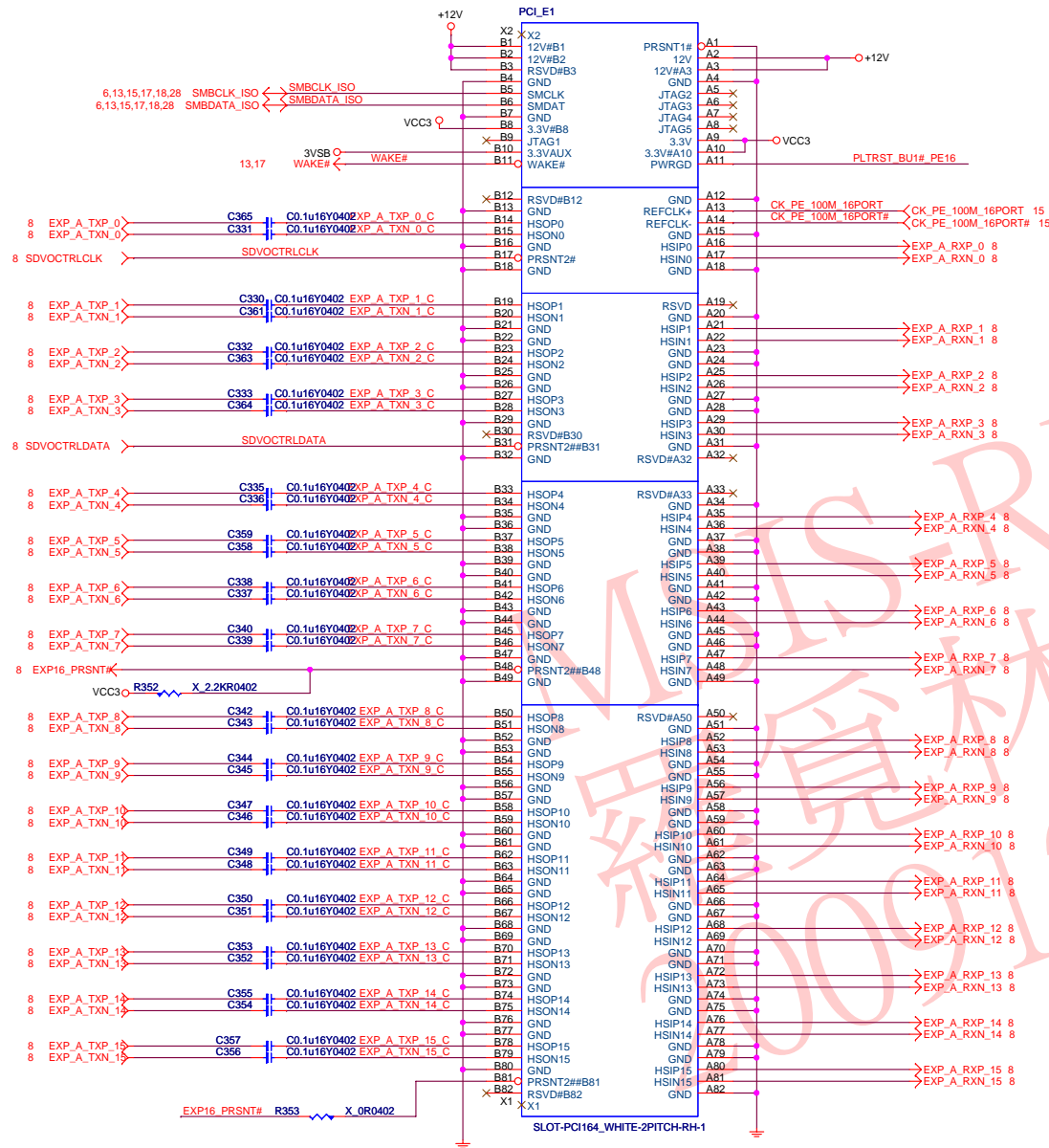


CHANNEL B V_SM_VTT DECOUPLING CAPS

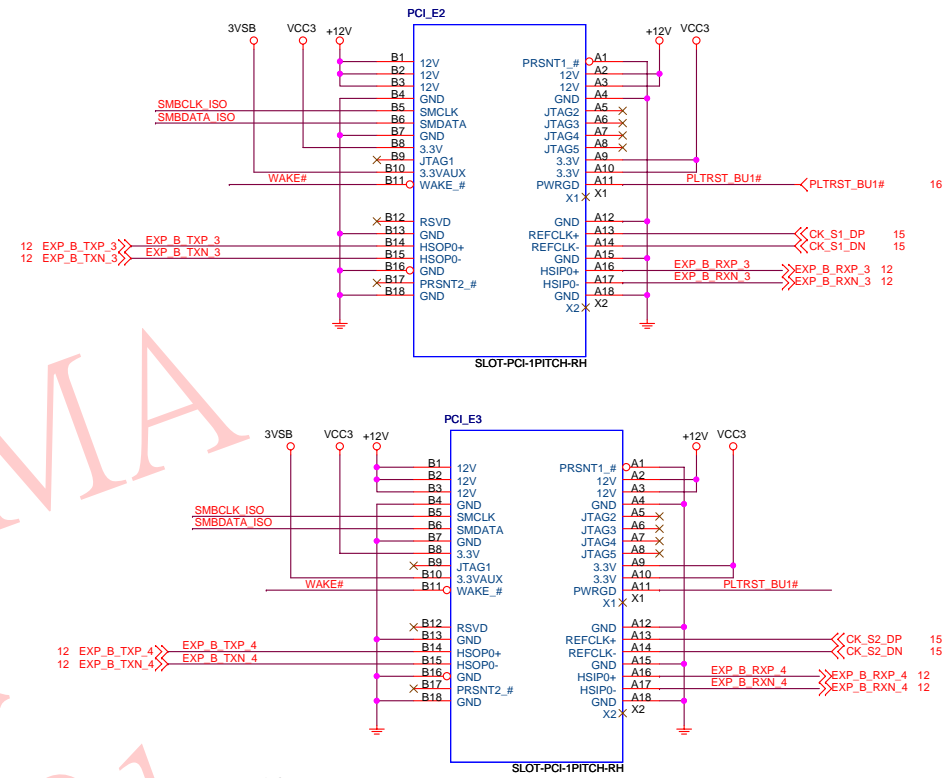


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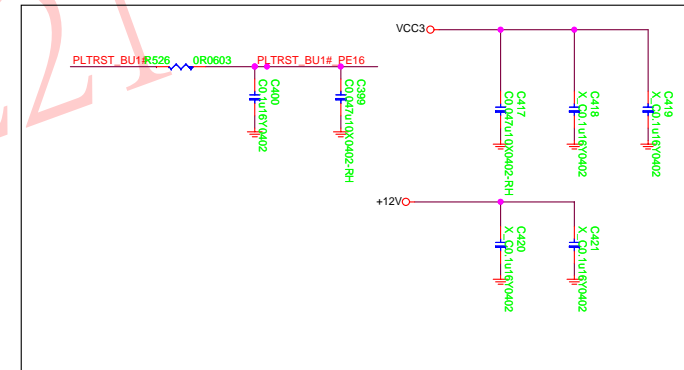
PCIE X16 PORT



PCIE X1 PORT



NEAR PCIE X16 SLOT

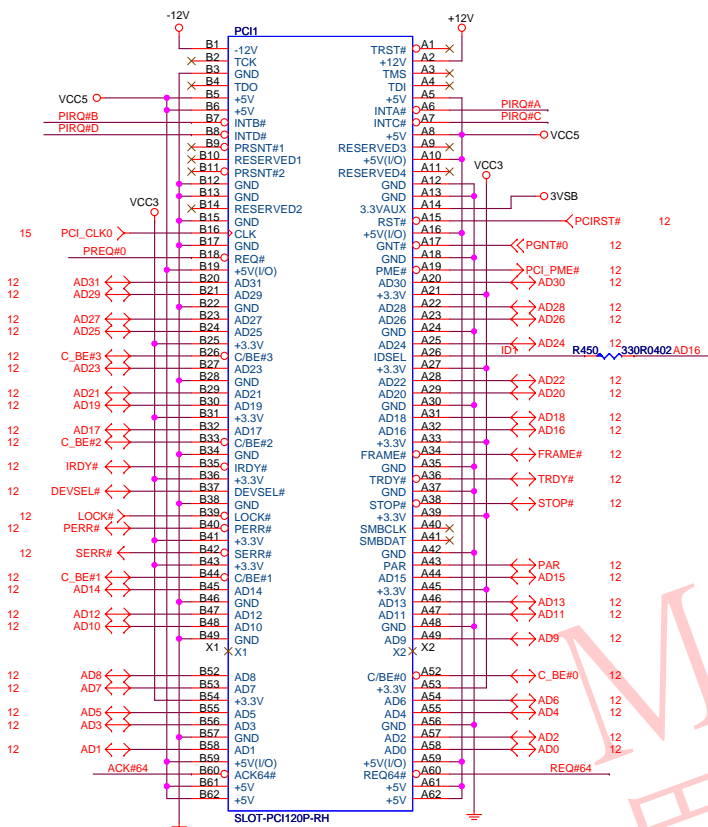


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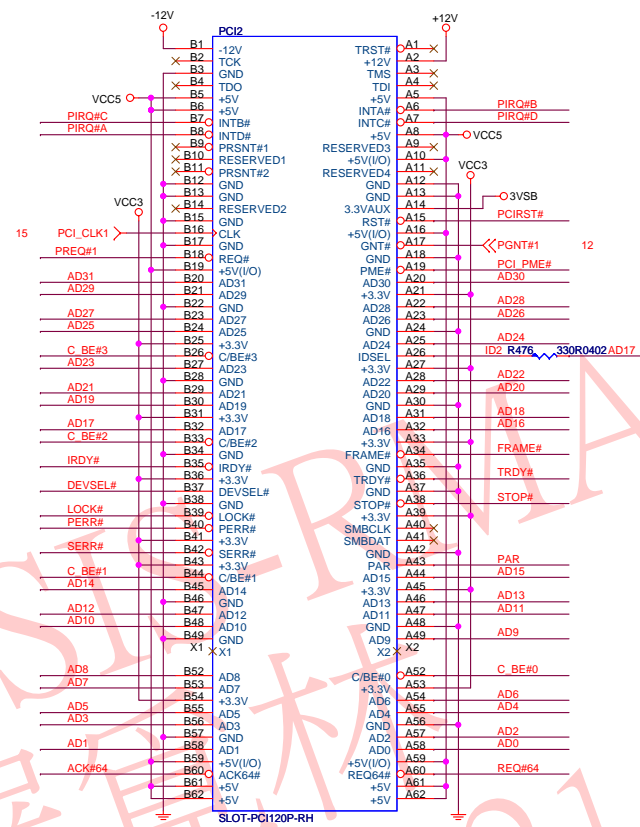
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PCI SLOT 1 (PCI VER: 2.2 COMPLY)



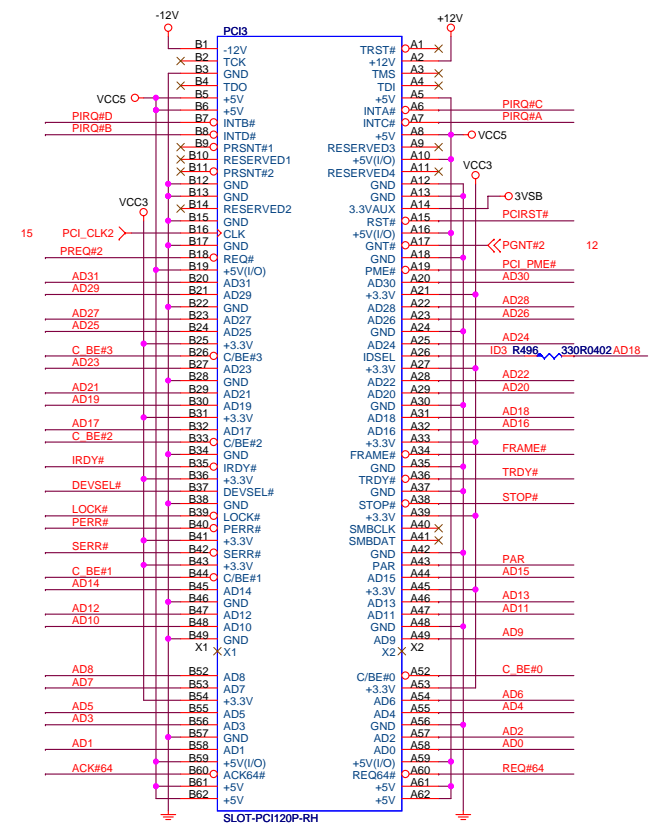
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



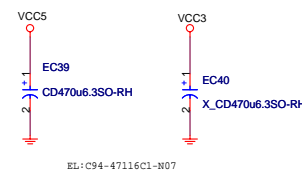
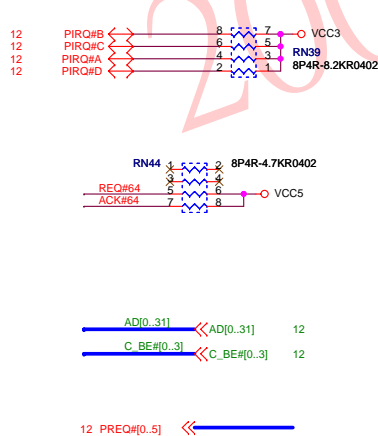
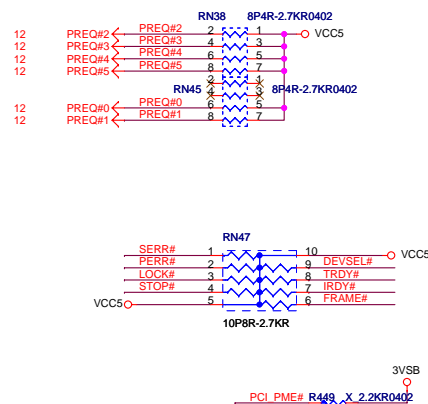
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI SLOT3 (PCI VER: 2.2 COMPLY)



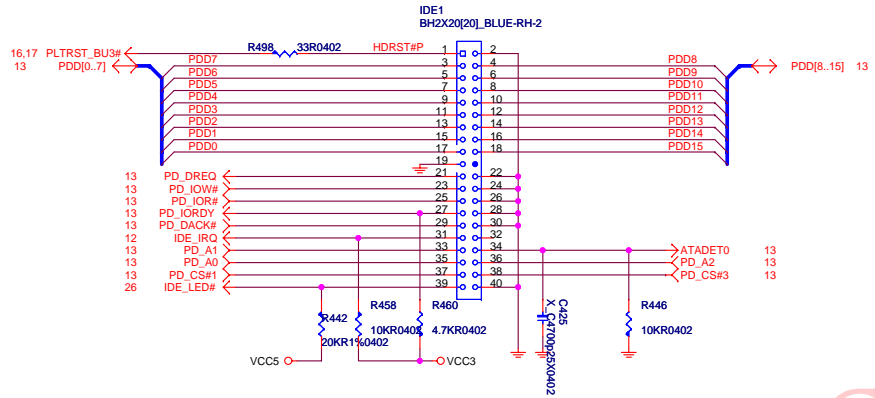
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS

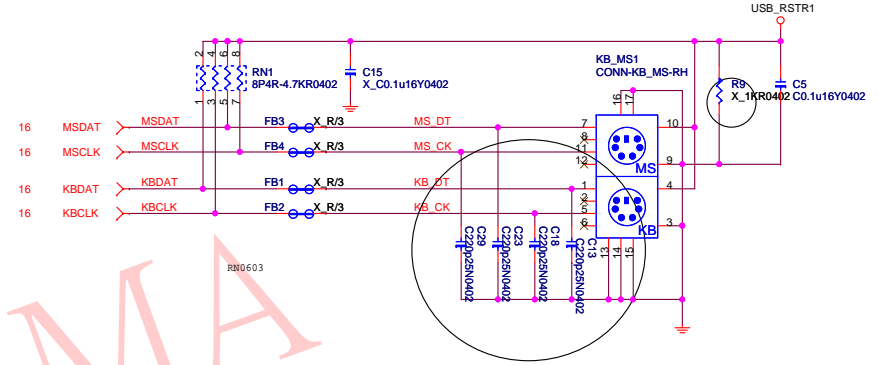


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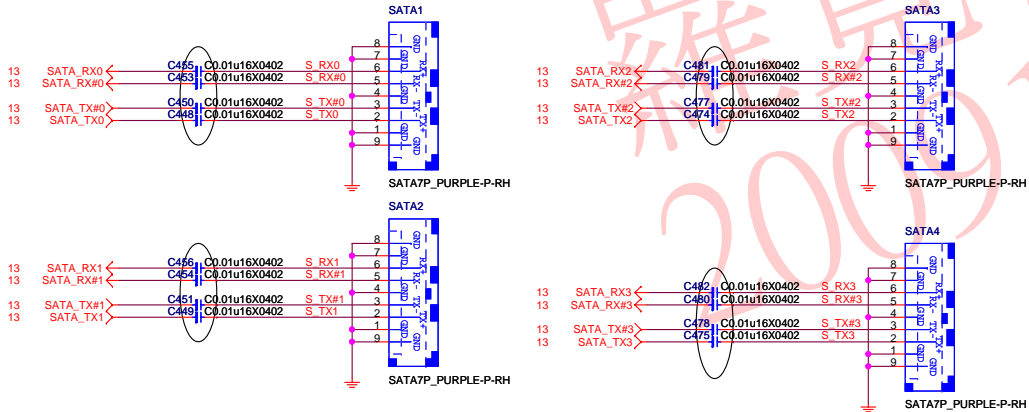
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



MICRO-STAR INT'L CO.,LTD

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29

VCC5 0 5VSB

C487
X_C10u10Y0805

U27

1 2 3 4 5 6 7 8

S3# 5VCC 5VSB VOUT1

OC# 5VCC 5VSB VOUT2

EN GND

USB_DRV ↔ USB_DRV

13 USB_OCP#3 <<

USB_EN

USB_FSTR1

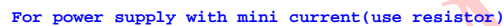
UP7533AM8_SOT23-8-RH

[illegible][illegible][illegible]

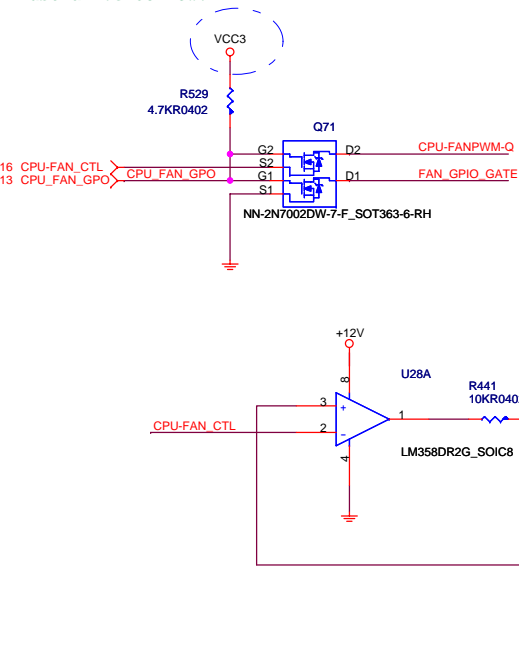
MS-7610

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ATX Connector



CPU FAN



INTEL/PB Front Panel Connector

The diagram illustrates the wiring for the Intel/PB Front Panel Connector. Key components and connections include:

- Connectors:** JFP1 (Front Panel Connector), N31-2051421-H06 (Motherboard Connector).
- Resistors:**
 - 330R: Connected between VCC5 and SATA_LED#.
 - 10KR0402: Connected between VCC3 and FP_RST#.
 - 4.7KR0402: Connected between 3VSB and PLED/SLED.
 - 4.7KR0402: Connected between PSIN and ground.
- Capacitors:**
 - C482, C489, C488: 10µF electrolytic capacitors connected to ground.
 - C486, C487: 10µF electrolytic capacitors connected to ground.
- Wiring:**
 - SATA_LED# (Pin 13) to JFP1 Pin 1.
 - IDE_LED# (Pin 24) to JFP1 Pin 2.
 - VCC5 (Pin 13, 15, 16, 28, 29) to JFP1 Pin 3.
 - VCC3 (Pin 13, 15, 16, 28, 29) to JFP1 Pin 4.
 - FP_RST# (Pin 13, 15, 16, 28, 29) to JFP1 Pin 5.
 - HDD+ (Pin 13, 15, 16, 28, 29) to JFP1 Pin 6.
 - HD_LED3 (Pin 13, 15, 16, 28, 29) to JFP1 Pin 7.
 - HDD- (Pin 13, 15, 16, 28, 29) to JFP1 Pin 8.
 - RESET- (Pin 13, 15, 16, 28, 29) to JFP1 Pin 9.
 - RESET+ (Pin 13, 15, 16, 28, 29) to JFP1 Pin 10.
 - NC (Pin 13, 15, 16, 28, 29) to JFP1 Pin 11.
 - PLED (Pin 13, 15, 16, 28, 29) to JFP1 Pin 12.
 - SLED (Pin 13, 15, 16, 28, 29) to JFP1 Pin 13.
 - PWSW+ (Pin 13, 15, 16, 28, 29) to JFP1 Pin 14.
 - PWSW- (Pin 13, 15, 16, 28, 29) to JFP1 Pin 15.
 - PSIN (Pin 13, 15, 16, 28, 29) to JFP1 Pin 16.

[illegible]

LED (for Fintek 71882)

The schematic diagram shows a fan speed control circuit. A +12V supply is connected to a network of resistors and a fan. Resistor R339 (4.7K) is connected between the +12V supply and a junction. From this junction, one path goes through resistor R342 (27K) to the SYS_FAN1 output, and another path goes to the fan. The fan, labeled SYSFAN2, has three terminals: terminal 3 is connected to the +12V supply, terminal 2 is connected to the junction after R339, and terminal 1 is connected to ground. A 16V battery (C310) is also connected to the junction after R339. Resistor R348 (10K) is connected between the SYS_FAN1 output and ground. The fan is identified as RH1X3B-FR_WHITE-RH.

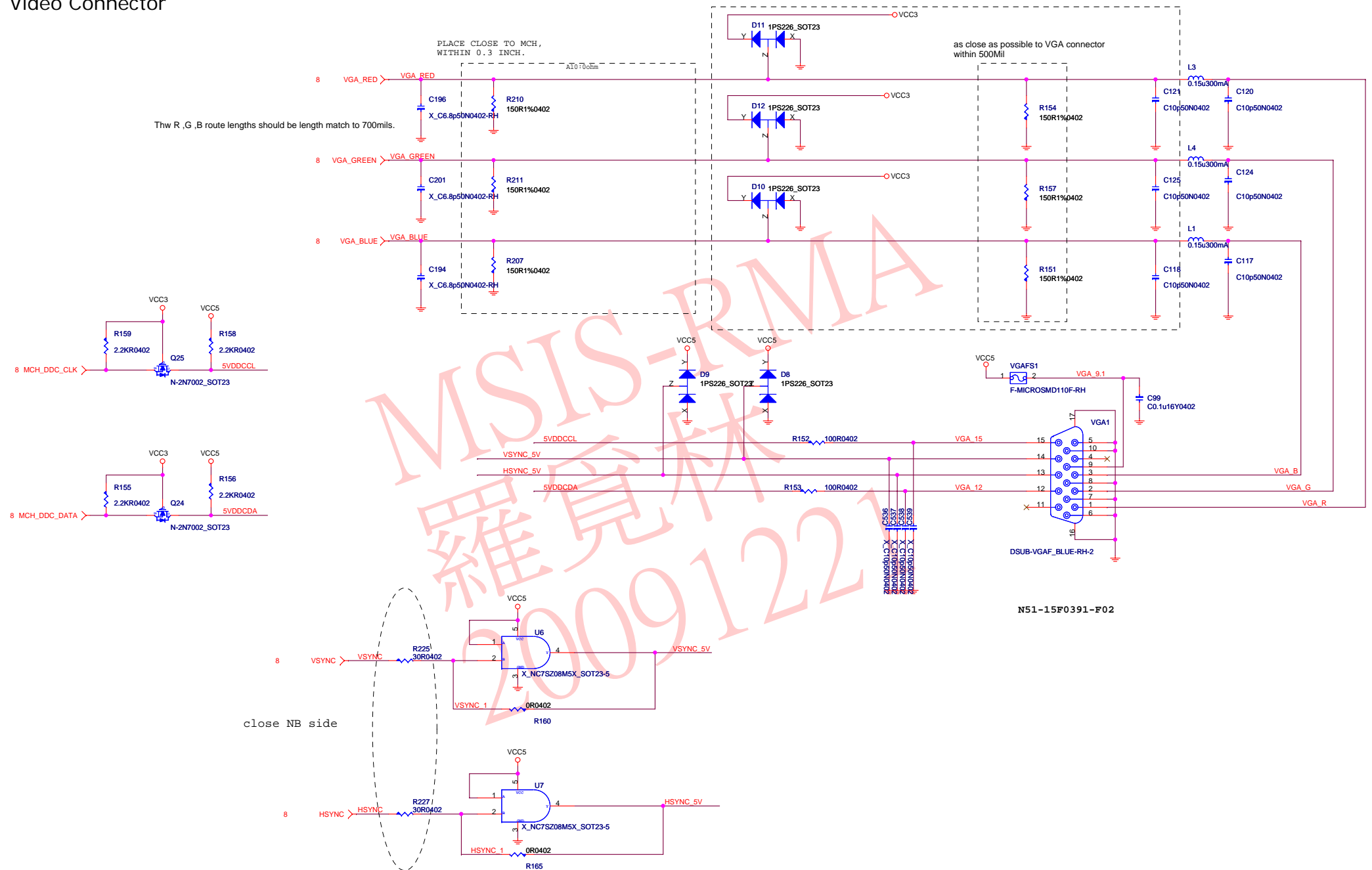
PWR FAN

The schematic diagram shows the PWR FAN circuit. A +12V supply is connected to a network of resistors and a fan. Resistor R341 (4.7KΩ) is in series with the +12V line. Resistor R344 (27KΩ) is connected between the line after R341 and the line after R349. Resistor R349 (10KΩ) is connected between the line after R344 and ground. The fan, SYSFAN1, is connected between the line after R341 and ground. The fan has three pins: 1 (blue), 2 (blue), and 3 (blue). The fan is labeled X_C10u16X51206-RH and H1X3B-FR_WHITE-RH.

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Video Connector

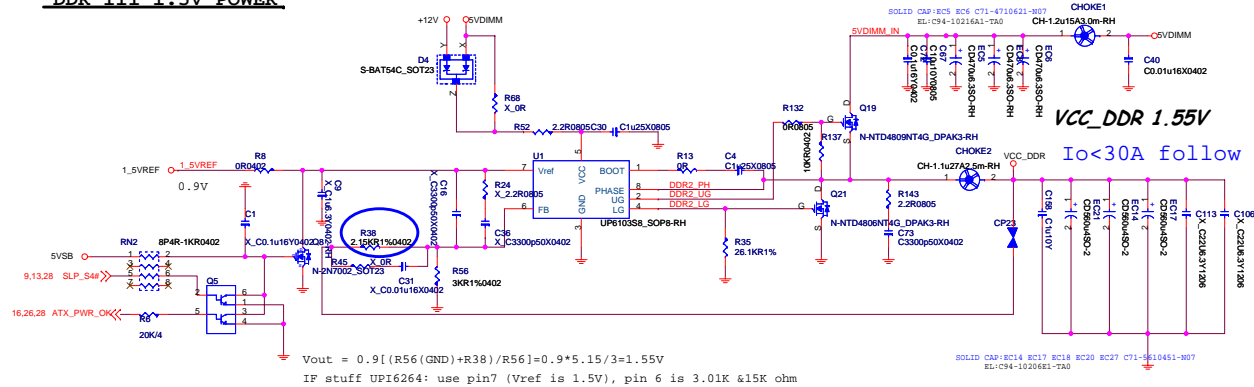


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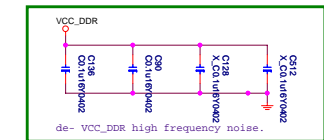
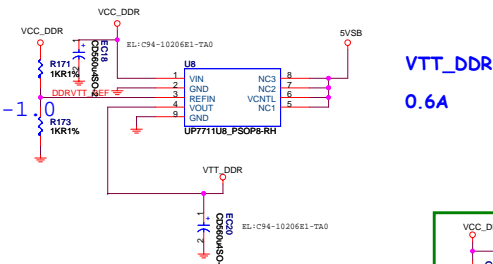
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DDR III 1.5V POWER

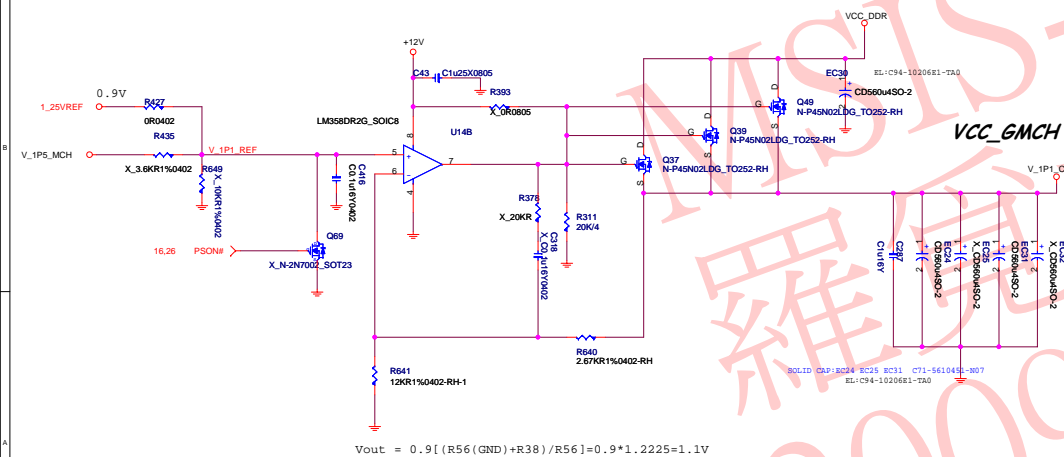


DDR VTT Power

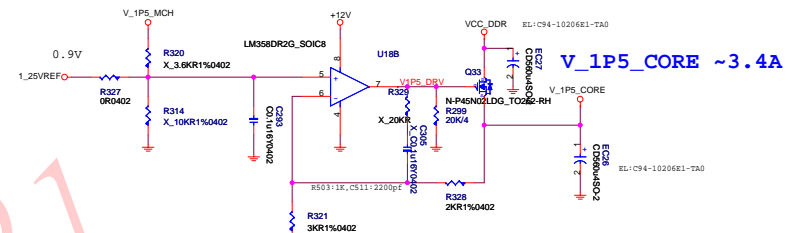
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MCH-G41 1.1V Core Power

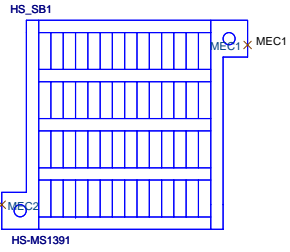


Design guide:22A
Run 3DMark:~14A max.
 $P_{min}=U \cdot I=(1.5V-1.1V) \cdot 14A=5.6W$
 $P_{dg}=U \cdot I=(1.5V-1.1V) \cdot 22A=8.8W$

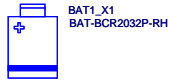
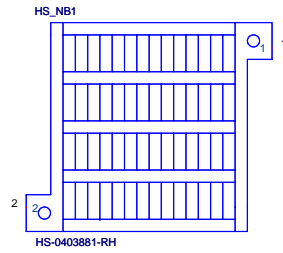
V 1P5 CORE

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ICH7 HEATSINK

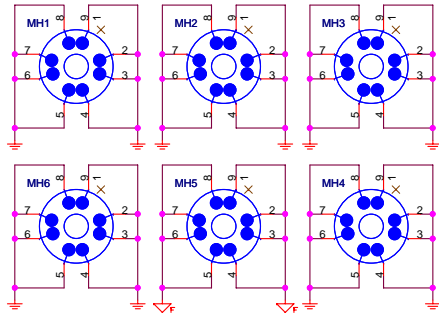


MCH HEATSINK

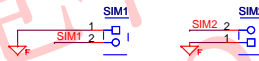


LABEL	PCB1	Rubber1	Rubber2	OPT1	OPT2	OPT8	OPT3	OPT5	OPT6	OPT7	OPT9	OPT10	OPT14	OPT18
P41-C31	PCB	rubber1/2	rubber1/2	0R0402	10/100 LAN CONR	J45_USBX2_LED	0R0402	0R0603CD470u16EL11.5-RH-5	0R0603CD470u16EL11.5-RH-1	CD1000u16EL20	CD1000u6.3EL11.5-RH-1	CD100u25EL11-RH-2	heatpipe	HEATSINK HS0404690-RH

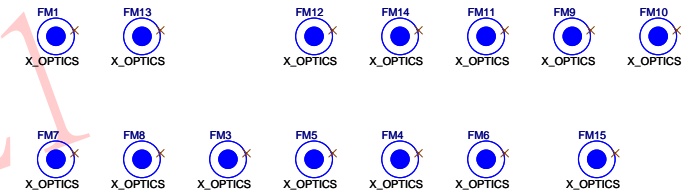
Mounting Holes



Simulation



Optics Orientation Holes



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ICH7								
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI GPIO(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO GPIO25(high 7507, low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.								

SIO Fintek71882FG(CONTINUE)					
GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICES	MCP1 INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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0A Change list:

1. Add pcie x1 *2,add one pci slot
- 2.change 1P1_core power mode
- 3.add APS function
- 4.modify Audio ALC888S circuit for realtek suggestion
- 5.add OC_SW1
- 6.add C14 C56 C61 C505 C506 C504 C370 for power supply with mini current(use resistor)
- 7.Update TO252 footprint to DPAKSGD
- 8.Add PLTRST#_R,EXP_RBIAS,SCL_A,SDA_A,SDA_LAN net name
- 9.add Q34 Q37 R315
- 10.For power:add C536 C509 C510 C511 R504 R315 R501 R591 R500 R503 R502 EC47

1.0 Change list:

1. switch CPU_BSEL0 to J_CPU_BSEL2
- 2.load power solution
- 3.add R515 R516 and update new solution for 5VDIMM
- 4.delete CN7 add C536-539
5. add R517 R518, follow msi-newheader_0216,change JPWR1 JPWR2 JCD1 KB_MS1
- 6.change EC20 footprint

2.0 Change list:

1. change print port to pinheader(page 16)
2. change DD2 to DDR3,add DRAMPWROK circuit(Page 09)
3. change GPIO06 function for USB_EN,GPIO21 for BOM
4. Add SIO Vref circuit(page 16)
5. Delete LANDSM_GPIO(page17)
- 6.Reserve R404 R395 for usb_en from SB(page 13)
- 7.add D2 for CPUFANCTL
- 8.Change NB POWER MODE
- 9.change Y3 footprint to OSCC_MS
- 10.add VCCGATE & DUALGATE circuit for 5VDIMM
11. change LAN chip to athros
- 12.Change audio chip to via,and add audio_gpio from ich7
- 13.Reserve R688,C806

2.1 Change list:

1. P16 ADD C400 C399 R526 R527 TO AVOID NV9600GSO VGA CARD RUN 3D FAIL.
2. P28 RESERVE PATCH 5VDIMM DROP CICUIT.
3. P21 UPDATE CIS ABOUT JSP1
4. P16 SWAP PLTRST_BU2# AND PLTRST_BU1#.

Title		
History		
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